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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,323	08/24/2001	Wei-Yung Hsu	AMAT/5617/CMP/CMP/RKK	3877

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APPLIED MATERIALS, INC.
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SANTA CLARA, CA 95050

EXAMINER	
KUNEMUND, ROBERT M	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,323	HSU ET AL.	
	Examiner	Art Unit	
	Robert M Kunemund	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 40-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 40-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim1 to 11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no teaching or suggestion is the originally filed specification that the first etching step is to be "selective" as is now claimed. The specification teaches etching in the first step and does not teach selectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al '223 (6,225,223).

Applicant discloses a method for processing a substrate comprising providing a substrate having feature definitions formed in a dielectric material, depositing a barrier layer material on the substrate surface and within the feature definitions, depositing a first conductive layer on the barrier layer to fill the feature definitions, polishing the first conductive material to at least the top surface of the barrier layer material, depositing a second conductive material by an electrochemical deposition technique to fill recesses formed in the first conductive material, and polishing the second conductive material to at least the top surface of the dielectric layer to form a planar surface. Applicant further claims various conductive materials that may be used as the first and second conductive materials, one of the claimed materials being copper.

Liu et al, '223, disclose a method for eliminating dishing of copper interconnects by forming a dielectric layer on a semiconductor substrate, forming trenches within the dielectric layer, depositing a barrier layer over the dielectric layer thereby lining the trench, depositing copper on the barrier layer to form a first copper layer filling the lined trench, planar zing the first copper layer and barrier layer thereby re-exposing the upper surface of the dielectric layer but also dishing the copper-filled trench, and selectively depositing copper on the dished copper-filled trench to form a second copper layer over the dished-copper-filled trench and extending above the upper surface of the dielectric layer. Liu et al, '223, additionally discloses that the second copper layer may be deposited by electroless plating or electrochemical deposition and that the second

copper layer may be planarized to form an essentially planar copper interconnect (claim 4). Liu et al, '223, disclose that a copper seed layer may also be deposited on the barrier layer prior to the deposition of the first copper layer (column 3, lines 30-36). Liu et al, '223, also disclose that the dielectric layer is between 4000 and 10,000 A thick with the barrier layer being between 100 and 500 A thick and the first copper layer being between 1000 and 2500 A thick. Deposition of the second copper layer to a thickness of 2000 A will result in the upper surface of the second copper layer extending above the upper surface segments of the dielectric layer prior to the planarization thereof. The sole difference between the instant claims and the prior art is the elective etching. However, in the absence of unexpected results, it would have been obvious to one of ordinary skill in the art to determine through routine experimentation, the optimum, operable etch type in the Liu et al "223 reference in order to remove only the material desired which in turns produces more uniform layers.

Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al,'223, as applied to claim 1 above, and further in view of Iacoponi et al. Liu et al, '223, teach the above method for depositing and polishing various layers on a semiconductor substrate to form conductive interconnects but does not teach the use of annealing or rinsing steps nor the use of a manufacturing system having multiple processing stations.

Iacoponi et al teach annealing of a deposited copper trench-fill layer to control the mechanical stress of the deposited copper layer (column 6, lines 23 – 46). Iacoponi et al also teach the use of a manufacturing system having multiple stations (column 9, line 58 - column 10, line 4) with the additional of intermediate processing steps including rinsing (column 9, line 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the annealing and rinsing steps taught by Iacoponi et al in the process taught by Liu so that the mechanical stresses and quality of the resulting conductive interconnects would be improved.

Claims 11 – 17 and 40 to 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al, '223, in view of Iacoponi et al, and further in view of Zhang.

Liu et al, '223, teach the above method for depositing and polishing various layers on a semiconductor substrate to form conductive interconnects. Iacoponi et al teach the above method for forming conductive interconnects including steps for annealing and rinsing the workpiece and also the use of a manufacturing system having multiple stations for performing the various process steps, however neither reference teaches the concurrent deposition and polishing of a conductive layer.

Zhang teaches a method for concurrent deposition and polishing of a conductive layer which facilitates the efficient manufacture of electrical interconnections between components of an integrate circuit.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the concurrent deposition and polishing method taught by

Zhang in the process taught by the combination of Liu and Iacoponi to improve the efficiency of the process for forming conductive interconnects.

Applicant's arguments filed February 9, 2004 have been fully considered but they are not persuasive.

Applicants' argument concerning the Liu et al reference is noted. However, the reference teaches the polishing of a first metal, copper, and then a second deposition to fill the trench with a metal. The second metal is then polished or planarized. This meets the claimed steps. Further, selective etching is well with in the skill of the art.

Applicants' argument concerning the Iacoponi et al reference has been considered and not deemed persuasive. The Iacoponi et al reference does not have to show the first and second deposition steps in order to meet the claims. The Liu et al reference already sets forth those steps and is modified by the teachings of the iacoponi et al reference concerning the use of annealing and rinsing in improving the processing and formation of devices.

Applicants' argument concerning the Zhang et al reference is noted. However, the Zhang et al reference is relied on to show the art conventionality of the concurrent steps of deposition and polishing. The reference modifies the Liu et al reference by teachings the improvements of the concurrent processing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert M Kunemund whose telephone number is 571-272-1464. The examiner can normally be reached on 8 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMK

ROBERT KUNEMUND
PRIMARY EXAMINER